CHANGES TO THE SPECIFICATION

Please substitute the following marked up paragraph(s) for the paragraph(s) now appearing in the currently filed specification:

Paragraph beginning at page 1, line 16:

FIG. 18 is a plan view showing the configuration of a conventional variable frequency band-pass filter 1. FIG. 19 is an electric circuit diagram of the band-pass filter of FIG. 18. The filter 1 comprises resonance circuits coupled in two stages, and comprises dielectric resonators 2 and 3, coupling capacitors C5, C6 and C7, polarization capacitors C1 and C2 for producing an attenuation pole, frequency shifting capacitors C3 and C4, PIN diode D1 and D2 as reactance elements, inductors L1 and L2 to function as choke coils, control voltage supply resistors R1 and R2, capacitors C8 and C9, and a circuit substrate 5 (Fig. 18) for mounting these parts. Moreover, an input terminal electrode P1, an output terminal electrode P2, voltage control terminal electrodes CONT1 and CONT2, and ground patterns G1 and G2 are shown in FIG. 18.

Paragraph beginning at page 5, line 18:

Moreover, according to the present invention, there is provided a dielectric filter which comprises a dielectric block having at least one resonance hole, a conductor inserted into the resonance hole while the conductor is insulated from an inner conductor of the resonance hole, a voltage-controllable reactance element electrically connected to the conductor, and a circuit substrate for the reactance element to be mounted onto, disposed on an outer face of the dielectric block excluding the under face thereof. ~~Thereby~~ Therefore, the inner conductor of the resonance hole and the conductor inserted into the resonance hole form a frequency shifting capacitor. Thus, it is unnecessary to provide a conventional frequency shifting capacitor element.

Paragraph beginning at Page 6, line 7:

Moreover, according to the present invention, there is provided a dielectric filter comprising a dielectric block having at least one resonance hole, a conductor electrically connected to an inner conductor of the resonance hole, a voltage-controllable reactance element electrically connected to the conductor, and a circuit substrate for the reactance element to be mounted onto, disposed on an outer face of the dielectric block excluding the under face thereof. Onto the circuit substrate, a circuit element for controlling the frequency shifting capacitor element and the reactance element, and so ~~froth~~ forth may be mounted in addition to the reactance elements.

Paragraph beginning at Page 16, line 17:

The pass frequency of the dielectric filter 11 is determined by the resonance frequency of a resonance system comprising the frequency shifting capacitor Cs1 and the dielectric resonator R1 and that of a resonance system comprising the frequency shifting capacitor Cs2 and the dielectric resonator R2. That is, when a positive control voltage is applied to the voltage control terminal electrode 23, the PIN diodes D11 and D12 are turned on. Accordingly, as shown in FIG. 3, the frequency shifting capacitors Cs1 and Cs2 are grounded via the PIN diodes D11 and D12 (not shown in FIG. 3), respectively, so that the pass frequency is decreased. At this time, the coupling adjustment capacitor C11 exerts no influence, since it is grounded. The dielectric resonators R1 and R2 are coupled to each other via electromagnetic coupling K. Thus, the pass bandwidth of the dielectric filter 11 is set.

Paragraph beginning at Page 17, line 8:

To the contrary, when a negative voltage is applied as a control voltage to the voltage control terminal electrode 23, the PIN diodes D11 and D12 are (not shown in FIG. 3) are turned off. Thereby, as shown in Fig. 4, the frequency shifting capacitors Cs1

and Cs2 become open, and the pass frequency is increased. Then, the dielectric resonators R1 and R2 are coupled to each other via the electromagnetic field coupling K and the capacitive coupling caused by the frequency shifting capacitors Cs1 and Cs2, and the coupling adjustment capacitor C11. Accordingly, the pass bandwidth obtained when the PIN diodes D11 and D12 are off and that obtained when the PIN diodes D11 and D12 are on can be set independently with a reduced number of parts and a small current consumption.

Paragraph beginning at Page 26, line 6:

Accordingly, the dielectric filter 71 has substantially the same equivalent circuit as that of the electric circuit shown in FIG. 2 ~~excepting~~ except that the coupling adjustment capacitor C11 is excluded. As a result, the dielectric filter 71 can be reduced in size. The height of the filter 71 can be even more reduced as compared with the filter 51 of the fourth embodiment.

Paragraph beginning at Page 27, line 15:

In the dielectric filter 91 having the above-described configuration, the frequency shifting capacitor Cs1 is formed by generation of an electrostatic capacitance between the metallic pin 95 and the inner conductor 16 of the resonance hole 13. The frequency shifting capacitor Cs2 is formed by generation of an electrostatic capacitance between the metallic pin 94 and the inner conductor 16 of the resonance hole 14. Thus, the frequency shifting capacitors Cs1 and Cs2 have the structure of a so-called coaxial capacitor, and therefore, have a large electrostatic capacitance, respectively. The dielectric capacitor 91 has substantially the same equivalent circuit as that of the electric circuit of FIG. 2 ~~excepting~~ except that the coupling adjustment capacitor C11 is excluded.

Paragraph beginning at page 29, line 7:

The circuit substrate 80 is arranged so as to be opposed to the opening end-face 12a of the dielectric block 12. The heads of the connecting members 102 and 103 are soldered to the relay electrode patterns 81a and 82a formed on the back side of the circuit substrate 80. On the front side of the circuit substrate 80, the relay electrode patterns 81, 82, 88a, and 88b, the voltage control electrode pattern 86, ~~and the voltage control electrode pattern 86~~, and the ground patterns 89a and 89b are provided. To the circuit substrate 80, the chip capacitors Cs1 and Cs2 as the frequency shifting capacitors are mounted, in addition to the PIN diodes D11 and D12 and the inductors L11 and L12.

Paragraph beginning at Page 29, line 22:

The eighth embodiment is substantially the same as the first embodiment ~~excepting~~ except that a concavity 112 is provided, instead of the step 18 of the dielectric filter 11 of the first embodiment. As shown in FIG. 11, in the variable frequency dielectric filter 111, the concavity 112 is formed on the upper face 12c of the dielectric block 12.

Paragraph beginning at Page 30, line 3:

The two separated electrodes 24 and 25, together with a part of the outer conductor 17 and the voltage control terminal electrode 23, are formed in the concavity 112 on the upper face 12c of the dielectric block 12 so as not to be electrically connected2.oo the outer conductor 17 and the other electrodes 21, 22 and ~~to~~ 23. In the concavity 112, the PIN diodes D11 and D12, and the inductors L11 and L12 are mounted. The PIN diode D11 is electrically connected between the outer conductor 17 and the separated electrode 24. The PIN diode D12 is electrically connected between the outer conductor 17 and the separated electrode 25. The inductor L11 is electrically connected between the separated electrodes 24 and 25 in parallel to them. The inductor

L12 is electrically connected between the separated electrode 25 and the voltage control terminal electrode 23.

Paragraph beginning at Page 31, line 12:

As shown in FIG. 12, the variable frequency band-pass dielectric filter 121 is substantially the same as the dielectric filter 11 of the first embodiment, ~~excepting~~ except that the PIN diodes D11 and D12 are mounted in the resonance holes 13 and 14, respectively. Concretely, the outer conductor 17, the input terminal electrode 21, the output terminal electrode 22, and the separated electrodes 24 and 25 are formed on the outer face of the single dielectric block 12 having a substantially rectangular parallelepiped shape. A step 18 is formed on the upper face 12c of the dielectric block 12. The inductors L11 and L12 are mounted on the lower portion 19 of the upper face 12c. Furthermore, the PIN diodes D11 and D12 are formed in the resonance holes 13 and 14. For the purpose of mounting the PIN diodes D11 and D12, the hole diameters at the opening end-face 12a of the resonance holes 13 and 14 are set to be larger than those at the short-circuited end-face 12b thereof.

Paragraph beginning at Page 32, line 26:

The PIN diode D11 (not shown in FIG. 14) is electrically connected between the outer conductor 17 and the separated electrode 24 in the resonance hole 13. The PIN diode D12 (not shown in FIG. 14) is electrically connected between the outer conductor 17 in the resonance hole 14 and the separated electrodes 25 in the resonance hole 14. The inductor L11 (not shown in FIG. 14) is electrically connected between the separated electrodes 24 and 25. The inductor L12 (not shown in FIG. 14) is electrically connected between the separated electrode 25 and the voltage control terminal electrode 23.

Paragraph beginning on Page 33, line 25:

As shown in FIG. 15, the tenth embodiment is the same as the second embodiment, ~~excepting~~ except that a concavity 132 is formed on the opening end-face 12a of the dielectric block 12 of the dielectric filter 31.

Paragraph beginning on Page 36, line 6:

FIG. 17 is an electric circuit block diagram of the RF part of a portable telephone 150. In FIG. 17, an antenna element 152, a duplexer 153, a transmission side isolator 161, a transmission side amplifier 162, a transmission side interstage band-pass filter 163, a transmission side mixer 164, a reception side amplifier 165, a reception side interstage band pass filter 166, a reception side mixer 167, a voltage control oscillation device (VCO) 168, and a local band-pass filter 169 are shown.